


11/06/00
13603 U.S. PTO



Please type a plus sign (+) inside this box 

PTO/SB/05 (12/97)
Approved for use through 9/30/00 OMB 0651-0032
Patent and Trademark Office U S DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

13614 U.S. PTO
09/705729
11/06/00

| | | | | |
|---|----------------------------------|---|------|------------------|
| Utility Patent Application Transmittal <small>(only for nonprovisional applications under 37 CFR 1.53(b))</small> | Attorney Docket No. | OKI 267 | Date | November 6, 2000 |
| | Inventor (s) : Yoshinori SHIZUNO | | | |
| | TITLE: | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME | | |

| | | | | | |
|---|--|--|----------------|---------|----------------|
| APPLICATION ELEMENTS See MPEP chapter 600 concerning utility patent application contents. | Assistant Commissioner for Patents ADDRESS TO: Box Patent Application Washington, DC 20231 | | | | |
| <p>1. <input checked="" type="checkbox"/> Patent Application Fee Determination Record (Submit an original, and a duplicate for fee processing)</p> <p>2. <input checked="" type="checkbox"/> Specification [Total Pages 25] (preferred arrangement set forth below)</p> <ul style="list-style-type: none">- Descriptive title of the Invention- Cross References to Related Applications- Background of the Invention- Brief Summary of the Invention- Brief Description of the Drawings (if filed)- Detailed Description- Claim(s)- Abstract of the Disclosure <p>3. <input checked="" type="checkbox"/> Drawing(s) Figures 1-8 [Total Sheets 6]</p> <p>4. Oath or Declaration [Total Sheets 3] <input checked="" type="checkbox"/> Newly executed (original or copy)</p> | | ACCOMPANYING APPLICATION PARTS <p>8. <input checked="" type="checkbox"/> Assignment & Recordation Cover Sheet [Total pages 3]</p> <p>9. <input type="checkbox"/> Information Disclosure Statement (IDS)/PTO-1449 [Total Pages] [Total References]</p> <p>12. <input type="checkbox"/> Preliminary Amendment [Total Pages]</p> <p>13. <input checked="" type="checkbox"/> Return Receipt Postcard (MPEP 503)</p> <p>14. <input type="checkbox"/> Small Entity Assertion</p> <p>15. <input checked="" type="checkbox"/> Certified Copy of Priority Document(s) The rights of priority are claimed under 35 U.S.C. § 119 of Japanese Application No. 320442 Filed 11 November 1999</p> <p>16. <input type="checkbox"/> Other: _____</p> | | | |
| 18. CORRESPONDENCE ADDRESS | | | | | |
| If there is no check attached, or the check is made out for an insufficient amount,  deficiency to our Deposit Account No. 18-0002 and notify us accordingly. | | | | | |
|  23995 PATENT TRADEMARK OFFICE | | | | | |
| NAME | Steven M. Rabin (Reg. No. 29,102) - Rabin & Champagne, P.C. | | | | |
| ADDRESS | 1101 14 th Street, N.W. Suite 500 | | | | |
| CITY | Washington | STATE | D.C. | ZIPCODE | 20005 |
| COUNTRY | USA | TELEPHONE | (202) 659-1915 | FAX | (202) 659-1898 |

+

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Box CPA, Washington, DC 20231.

SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

Field of the Invention:

The present invention relates to a semiconductor device and a method of manufacturing the same, and particularly to a semiconductor device and a manufacturing method thereof capable of improving control on foam developed upon curing an encapsulating resin.

This application is a counterpart of Japanese Patent Application, Serial Number 320442/1999, filed November 11, 1999, the subject matter of which is incorporated herein by reference.

Description of the Related Art:

With recent high-density mounting, a semiconductor device designed in a BGA (Ball Grid Array) package described in, for example, Japanese Patent Application Laid-Open No. Hei 11-97567, wherein ball-shaped solder terminals are placed over a board or substrate mounting surface of the package in grid form, has come on the stage. With high-speed and high integration of an LSI, there has been an increasing demand for improvements in electric characteristics and heat dissipation property with respect to package mounting or implementation.

As one measure taken against it, there has been proposed a cavity down type BGA package wherein ground and power planes are placed over a multilayer printed

circuit board to improve electric characteristics and a heat spreader is provided over a chip mounting surface to thereby enhance a heat dissipation property.

Fig. 8 is a cross-sectional view showing a semiconductor device designed in a conventional cavity down type BGA package.

This type of semiconductor device includes a semiconductor chip 1 on which although not illustrated in the drawing, circuits and bonding pads are formed, a multilayer wiring substrate or board 2 on which although not shown in the drawing, bonding posts, circuits and through holes are formed in positions corresponding to the respective pads, a heat spreader 3 to which the semiconductor chip 1 and the wiring board 2 are fixed, metal thin wires 4 for connecting the pads and the posts respectively, and an encapsulating resin 5 for sealing the parts inclusive of the semiconductor chip 1 and the metal thin wires 4.

Solder balls 6 used as external terminals and a dam 7 are provided over the wiring board 2. Further, an opening for holding or accommodating the semiconductor chip 1 is defined in the wiring board 2. Although not shown in the drawing, the wiring board 2 is provided with ground and power planes for improving electric characteristics.

The semiconductor chip 1 is fixedly secured to the heat spreader 3 through the opening defined in the wiring

board 2 with a die attach material 8 interposed therebetween. The wiring board 2 is fixedly secured to the heat spreader 3 with an adhesive 9. An organic adhesive is normally applied to the die attach material 8.

The encapsulating resin 5 such as an epoxy resin is charged up to an upper portion of the dam 7 and thereafter cured in a sealing process step. Afterwards, the solder balls 6 are fused so as to function as the external terminals respectively.

Defoaming is performed as needed upon charging of the encapsulating resin 5 to break or vanish foam which remain in the encapsulating resin 5, and a uniform sealed portion is formed after its curing, whereby a semiconductor device free of a reduction in reliability due to a moisture's trap or the like is completed.

Incidentally, reference numeral 10 indicates a recessed portion of the adhesive 9, and reference numerals 11 indicate voids.

Since, however, the wiring board 2 and the heat spreader 3 are fixedly secured to each other with the adhesive 9 in the conventional example, the size of the mountable semiconductor chip 1 was limited in consideration of an extended-out portion of the adhesive 9.

When the width of the adhesive 9 is rendered narrow to eliminate the extended-out portion of the adhesive 9 where clearance between the semiconductor chip 1 and the

wiring board 2 is less reduced due to the restriction that the body size of the package cannot be made great from a board mounting surface, and the reason of the electric characteristics of the metal thin wires 4, the recessed portion 10 is formed and foam are developed upon curing of the encapsulating resin. Thus, the foam remain as the voids 11 below narrow spatial portions of the metal thin wires 4, particularly in the neighborhood of the tops of the metal thin wires 4, whereby moisture resistance is reduced.

Further, a drawback arises in that even when the defoaming process step is introduced as a void measure, the volume of the recessed portion 10 becomes large and perfect defoaming is unfeasible, and a long time is required even if the defoaming becomes feasible, thereby causing a significant reduction in productivity.

SUMMARY OF THE INVENTION

In order to solve the above-described problems, there is provided first means wherein a semiconductor chip and a wiring board are fixed to a principal surface of a heat spreader by a layer composed of an adhesive.

There is provided second means wherein a layer composed of an adhesive having a thermal characteristic equivalent to the above adhesive is formed over a reverse surface of a heat spreader.

There is provided third means wherein a first

encapsulating resin is charged below portions of metal thin wires in which voids occur, exclusive of the portions thereof to eliminate a recessed portion, and a semiconductor chip is thereafter sealed with a second encapsulating resin.

Typical ones of various inventions of the present application have been shown in brief. However, the various inventions of the present application and specific configurations of these inventions will be understood from the following description.

BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming the subject matter which is regarded as the invention, it is believed that the invention, the objects and features of the invention and further objects, features and advantages thereof will be better understood from the following description taken in connection with the accompanying drawings in which:

Fig. 1 is a cross-sectional view showing a semiconductor device according to a first embodiment of the present invention;

Fig. 2 is a view illustrating a method of manufacturing the semiconductor device according to the first embodiment;

Fig. 3 is a cross-sectional view depicting a

semiconductor device according to a second embodiment of the present invention;

Fig. 4 is a view showing a method of manufacturing the semiconductor device according to the second embodiment;

Fig. 5 is a cross-sectional view illustrating a semiconductor device according to a third embodiment of the present invention;

Fig. 6 is a cross-sectional view depicting a semiconductor device according to a fourth embodiment of the present invention;

Fig. 7 is a cross-sectional view showing a semiconductor device according to a fifth embodiment of the present invention; and

Fig. 8 is a cross-sectional view illustrating a conventional semiconductor device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

First preferred embodiment:

Fig. 1 is a cross-sectional view showing a first embodiment of the present invention. The same elements of structure as those employed in the prior art shown in Fig. 8 are identified by the same reference numerals.

The semiconductor device has a semiconductor chip 1, a multilayered wiring substrate or board 2, a heat spreader 3, metal thin wires 4, and an encapsulating resin 5.

Unillustrated circuits and bonding pads are formed in the semiconductor chip 1.

The wiring board 2 has a square aperture or opening defined in its central portion and a cavity defined therein, which holds or accommodates the semiconductor chip 1 therein. Although not illustrated in the drawing, bonding posts are respectively formed in positions corresponding to the respective pads of the semiconductor chip 1, and circuits and through holes are formed so as to make electrical continuity between the posts and solder balls 6 which serve as external terminals.

A layer of an adhesive, i.e., an adhesive layer 12 is formed over the entire principal surface of the heat spreader 3. The wiring board 2 is fixed to the heat spreader 3 by the adhesive layer 12. Further, the semiconductor chip 1 is also fixed to the heat spreader 3 by the adhesive layer 12 through the above-described opening in a manner similar to above.

The semiconductor chip 1 and the wiring board 2 are electrically connected to each other by bonding the pads and posts to one another with the metal thin wires 4.

The semiconductor chip 1 and the metal thin wires 4 are encapsulated by filling the opening with the encapsulating resin 5 up to an upper portion of a dam 7. The solder balls 6 are fusioned after it has been cured.

Incidentally, the solder balls 6 can be omitted if solder joining is made possible by, for example, the

supply of soldering paste upon board mounting. Further, the dam 7 can be also deleted if the thickness of the wiring board 2 is sufficiently ensured and no metal thin wires 4 are exposed after encapsulation.

A B-staged thermosetting resin (whose curing has been stopped in the course thereof without reaching the final stage), a thermoplastic resin, a mixed material of the B-staged thermosetting resin and the thermoplastic resin, etc. can be applied to the adhesive layer 12.

For example, a B-staged epoxy resin used as the B-staged thermosetting resin needs care such as the need for cold storing processing to manage its reaction probability. However, the B-staged epoxy resin can be expected to have high adhesion. Further, the thermoplastic resin is easy to perform handling, and the mixed material has characteristics of the two referred to above.

While the semiconductor chip 1 is fixedly secured to the heat spreader 3 by the adhesive layer 12 other than the conventional die attach material, a high thermal-conductive adhesive is also known and can be also set to the same thermal conductivity as the die attach material. Even in the case of the die attach material and the adhesive, no serious influence occurs in terms of a heat dissipation property of a package.

According to the first embodiment as described above, since the semiconductor chip 1 and the wiring

board 2 are fixed to the heat spreader 3 by the adhesive layer 12 provided over the entire principal surface of the heat spreader 3, the conventional recessed portion of adhesive no occurs between the wiring board 2 and the heat spreader 3, so that voids can be prevented from occurring in an encapsulating process step.

Further, since no voids occur even if clearance between the semiconductor chip 1 and the wiring board 2 is reduced, the optimum structure can be brought about in which priority is given to electric characteristics such as the impedance characteristic of each metal thin wire 4, thus making it possible to implement a semiconductor device excellent in electric characteristics and moisture resistance.

Fig. 2 is a view illustrating a method of manufacturing a semiconductor device according to the first embodiment. Respective process steps are shown in the form of cross-sectional views.

A semiconductor chip 1, a wiring substrate or board 2 provided with an aperture or opening 13 for accommodating the semiconductor chip 1 therein and a dam 7, and a heat spreader 3 are first prepared.

In a process step (a), an adhesive layer 12 is formed over the entire principal surface of the heat spreader 3. An adhesive may be either a paste-like one or a sheet-like one.

In a process step (b), the wiring board 2 is

aligned with the heat spreader 3 with the adhesive layer 12 formed thereon. Thereafter, the wiring board 2 is fixed onto the principal surface of the heat spreader 3 by a method such as thermocompression bonding.

When the semiconductor chip 1 is fixed onto the principal surface of the heat spreader 3 formed with the adhesive layer 12 by the method such as the thermocompression bonding after the semiconductor chip 1 has been aligned through the opening 13 defined in the wiring board 2 in a process step (c), a state shown in a process step (d) is reached.

In a process step (e), pads used for the semiconductor chip 1 and posts used for the wiring board 2 are bonded to one another by metal thin wires 4 respectively. An encapsulating resin 5 is charged into the dam 7 up to its upper portion and then cured to thereby seal the parts inclusive of the semiconductor chip 1 and the metal thin wires 4. Thereafter, solder balls 6 are fusion-bonded, thus leading to completion of the first embodiment.

According to the method of manufacturing the semiconductor device according to the first embodiment as described above, since the semiconductor chip 1 and the wiring board 2 are fixed onto the principal surface of the heat spreader 3 by the adhesive layer 12 formed over the entire surface of the heat spreader 3, no conventional recessed portion occurs between the wiring

board 2 and the heat spreader 3 and voids can be prevented from occurring in the sealing process step. Thus, a defoaming process step becomes unnecessary and hence productivity is improved.

Further, since the adhesive layer 12 is used to fix the semiconductor chip 1, the conventionally-used die attach material becomes unnecessary. Although it was necessary to process the adhesive in frame form for fixing the wiring board, this process step can be deleted, thus leading to a reduction in cost.

Incidentally, since the portions cut when the adhesive is processed into frame form, are discarded, an increase in the adhesive to be used is limited by a portion corresponding to the non-need of the die attach material.

Second preferred embodiment:

Fig. 3 is a cross-sectional view showing a second embodiment of the present invention. The second embodiment is equivalent to one wherein a second adhesive layer 14 is further formed over the reverse surface of the heat spreader 3 in the first embodiment.

Since the second adhesive layer 14 is identical to the adhesive layer 12 formed over the principal surface of the heat spreader 3 in terms of a thermal characteristic such as a linear expansion coefficient, the same one may of course be used.

According to the second embodiment as described

above, since the adhesive layers 12 and 14 identical in thermal characteristic are formed over the principal surface and reverse side of the heat spreader 3 in addition to the effect obtained in the first embodiment, warpage can be reduced even if the heat spreader 3 and the adhesive layers 12 and 14 are different in thermal expansion characteristic from one another, thus making it possible to realize a semiconductor device wherein a wiring board 2 and the heat spreader 3 are good in adhesive property and a reduction in warpage is reached.

Fig. 4 is a view showing a method of manufacturing a semiconductor device according to the second embodiment. Respective process steps are shown in the form of cross-sectional views respectively.

A semiconductor chip 1, a wiring substrate or board 2 provided with an aperture or opening 13 and a dam 7, and a heat spreader 3 are first prepared.

In a process step (a), an adhesive layer 12 is formed over the entire principal surface of the heat spreader 3, and a second adhesive layer 14 is formed over the entire reverse surface of the heat spreader 3. An adhesive may be either a paste-like one or a sheet-like one. Further, different materials identical in thermal characteristic although identical in material quality may be used as the adhesive.

In a process step (b), the wiring board 2 is aligned with the heat spreader 3 with the adhesive layer

12 formed thereon. Thereafter, the wiring board 2 is fixed onto the principal surface of the heat spreader 3 with the adhesive layer 12 formed thereon, by a method such as thermocompression bonding.

When the semiconductor chip 1 is fixed onto the principal surface of the heat spreader 3 by the method such as the thermocompression bonding after the semiconductor chip 1 has been aligned through the opening 13 defined in the wiring board 2 in a process step (c), a state shown in a process step (d) is reached.

In a process step (e), the semiconductor chip 1 and the wiring board 2 are bonded to one another by metal thin wires 4 respectively. An encapsulating resin 5 is charged into the dam 7 up to its upper portion and then cured to thereby seal the parts inclusive of the semiconductor chip 1 and the metal thin wires 4. Thereafter, solder balls 6 are fusion-bonded, thus leading to completion of the first embodiment.

According to the method of manufacturing the semiconductor device according to the second embodiment as described above, since the second adhesive layer 14 can be formed over the reverse surface of the heat spreader 3 together with the process step for forming the adhesive layer 12 over the principal surface thereof in addition to the effect obtained by the method of manufacturing the semiconductor device according to the first embodiment, an additional adhesive and a process

step therefor are unnecessary when a radiating fin or the like is fixed to the reverse surface of the heat spreader 3, and the entire process can be simplified.

Third preferred embodiment:

Fig. 5 is a cross-sectional view showing a third embodiment of the present invention. The present embodiment is one wherein a radiating fin 15 is fixedly secured to the second embodiment.

The radiating fin 15 is fixed to a heat spreader 3 by a second adhesive layer 14 formed over the reverse surface of the heat spreader 3 according to a method such as thermocompression bonding.

According to the third embodiment as described above, the provision of the radiating fin 15 permits the enhancement of a radiation effect.

Fourth preferred embodiment:

Fig. 6 is a view showing a fourth embodiment of the present invention. Respective process steps are shown in the form of cross-sectional views respectively.

A semiconductor chip 1, a wiring board 2 provided with an opening 13 and a dam 7, and a heat spreader 3 are first prepared.

In a process step (a), a frame-shaped first adhesive layer 16 is formed over the principal surface of the heat spreader 3. The wiring board 2 is fixed to the heat spreader 3 with a first adhesive layer 16 interposed therebetween.

At this time, the first adhesive layer 16 is formed so as to become narrower than the wiring board 2 in width to avoid an extended-out portion thereof. However, a recessed portion 17 of an adhesive occurs due to such formation.

In a process step (b), a second adhesive layer 18 is formed over the principal surface of the heat spreader 3 through the opening 13 defined in the wiring board 2. Afterwards, the semiconductor chip 1 is mounted over the second adhesive layer 18. The process steps used until now are substantially the same as the conventional ones.

Incidentally, when a thermosetting resin is used as the second adhesive layer 18, it can be cured together in the following process step. It is thus possible to omit a curing process step for fixing the semiconductor chip 1.

In a process step (c), a first encapsulating resin 19 is charged into and cured within the opening 13 of the wiring board 2, which is located below bonding surfaces of the semiconductor chip 1 and the wiring board 2, i.e., the existing surfaces of both pads of the semiconductor chip 1 and posts of the wiring board 2 in such a manner that the recessed portion 17 is hidden. Namely, the second adhesive layer 18 and part of the semiconductor chip 1 are sealed with the first encapsulating resin.

Since the bonding surface of the wiring board 2 is lower than that of the semiconductor chip 1 in the present embodiment, the first encapsulating resin 19 is

charged up to a surface slightly lower than the bonding surface of the wiring board 2.

If done in this way, then no voids occur in the pads and posts requiring moisture resistance even if the recessed portion 17 is formed between the wiring board 2 and the heat spreader 3. The voids are developed only below the pads and posts. Since, however, the portion below them is cured, no influence is exerted on the reliability of the semiconductor device.

In a process step (d), the pads and posts are bonded to one another by metal thin wires respectively. Thereafter, a second encapsulating resin 20 is charged into the dam 7 up to its upper portion and then cured to thereby seal the parts inclusive of the semiconductor chip 1 and the metal thin wires 4. Incidentally, solder balls are omitted.

The first encapsulating resin 19 may satisfy sealing characteristics such as viscosity, curing speed, etc. at a temperature for charging the encapsulating resin. Alternatively, one identical in composition to the second encapsulating resin such as an epoxy resin may be selected.

If a filler having good thermal conductivity, e.g., an organic adhesive charged with silver is used for the second adhesive layer 18, then a heat dissipation property can be also improved.

According to the fourth embodiment as described

005074 02250600

above, the semiconductor chip 1 is placed over the principal surface of the heat spreader 3. Thereafter, the first encapsulating resin 19 is charged into and cured within the opening 13 located below the bonding surfaces of the semiconductor chip 1 and the wiring board 2, followed by bonding with the metal thin wires 4. Next, the parts are sealed with the second encapsulating resin 20 inclusive of the semiconductor chip 1 and the metal thin wires 4. Therefore, no voids occur in the pads and posts subjected to the wire bonding.

Further, since the members identical in structure to those employed in the conventional semiconductor device can be used, the effect of reducing the cost of each member can be expected owing to their standardization.

Fifth preferred embodiment:

Fig. 7 is a view showing a fifth embodiment of the present invention. Respective process steps are shown in the form of cross-sectional views respectively.

Since the present embodiment is identical to the fourth embodiment shown in Fig. 6 up to the process steps (a) and (b), their description will be omitted.

In a process step (c), pads provided within a semiconductor chip 1 and posts provided within a wiring board 2 are connected to one another by metal thin wires 4 respectively.

In a process step (d), a first encapsulating resin

21 is charged into and thereafter semi-cured within a lower opening 13 except for the neighborhood of the tops of the metal thin wires 4 at which voids are easy to remain, in such a manner that a recessed portion 17 is hidden.

One, which meets a sealing characteristic, may be used as the first encapsulating resin 21. Further, the semi-curing means that the first encapsulating resin 21 is cured up to viscosity corresponding to such an extent that at least the voids cannot be moved.

In a process step (e), a second encapsulating resin 22 is charged into a dam 7 up to its upper portion and then cured together with the first encapsulating resin 21 to thereby seal the parts inclusive of the semiconductor chip 1 and the metal thin wires 4. Incidentally, solder balls 6 are omitted.

Allowing the passage of the conventional sealer two times makes it possible to cope with the above-described semi-curing and curing process steps. Namely, the first encapsulating resin 21 is supplied in the first time and thereafter semi-cured in a heating zone of the sealer. In the second time, the second encapsulating resin 22 may be supplied and thereafter cured.

In this case, if the second encapsulating resin 22 has such a characteristic as to be sufficiently cured up to the viscosity corresponding to such an extent that at least the voids cannot be moved in the heating zone of

the sealer, the same one can be used for the first encapsulating resin 21 and the second encapsulating resin 22.

According to the fifth embodiment as described above, the semiconductor chip 1 is fixedly secured to the heat spreader 3 and subjected to bonding by the metal thin wires 4. Next, the first encapsulating resin 21 is supplied to and semi-cured within the lower opening 13 except for the neighborhood of the tops of the metal thin wires 4. Thereafter, the parts are sealed with the second encapsulating resin 22 inclusive of the semiconductor chip 1 and the metal thin wires 4. Therefore, the voids are developed only below the semi-cured first encapsulating resin 21, and no voids occur in the neighborhood of the tops of the metal thin wires 4 at which they are easy to remain, thereby exerting no influence on the reliability of the semiconductor device.

Since the encapsulation is done after the bonding using the metal thin wires 4 in the fifth embodiment, the pads become no dirty and a bad influence on wire bonding can be avoided, thus making it possible to improve the reliability of connections of the wiring portions.

While the present embodiment has been described with the cavity down type BGA package as an illustrative example, it can be similarly applied even to a BGA package of a type wherein a small heat spreader is bonded to a multilayer printed circuit or wiring board and

solder balls are provided on the heat spreader side, and an LGA (Land Grid Array) package with no solder balls mounted thereon.

No limitation is imposed on the multilayer wiring board. Even a single-layer wiring board and a double-sided wiring board can be embodied.

As described above, the present invention can implement a semiconductor device excellent in electric characteristics and moisture resistance because the recessed portion of the adhesive is eliminated and the voids are prevented from occurring, or the voids are encapsulated so as not to influence the portion requiring moisture resistance even if they occur.

While the present invention has been described with reference to the illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to those skilled in the art on reference to this description. It is therefore contemplated that the appended claims will cover any such modifications or embodiments as fall within the true scope of the invention.

WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:
a semiconductor chip;
metal thin wires respectively connected to
electrodes on said semiconductor chip;
a wiring board electrically connected to said
semiconductor chip by said metal thin wires;
a heat spreader equipped with said semiconductor
chip and said wiring board provided thereon;
an adhesive layer which is provided over a
principal surface of said heat spreader and bonds said
semiconductor chip and said wiring board to each other;
and
an encapsulating resin for sealing at least said
metal thin wires.
2. The semiconductor device as claimed in claim 1,
wherein a second adhesive layer having the same thermal
characteristic as said adhesive layer is provided over
the reverse surface of said heat spreader.
3. The semiconductor device as claimed in claim 2,
wherein a radiating fin is provided over said second
adhesive layer.
4. A method of manufacturing a semiconductor device,

comprising the following steps:

- a step for preparing a heat spreader;
- a step for forming an adhesive layer over a principal surface of said heat spreader;
- a step for forming a semiconductor chip and a wiring board over said adhesive layer;
- a step for connecting electrodes of said semiconductor chip and said wiring board by metal thin wires; and
- a step for sealing at least said metal thin wires with an encapsulating resin.

5. A method of manufacturing a semiconductor device, comprising the following steps:

- a step for preparing a heat spreader;
- a step for forming a first adhesive layer and a second adhesive layer over a principal surface of said heat spreader;
- a step for forming a wiring board over said first adhesive layer;
- a step for forming a semiconductor chip over said adhesive layer;
- a step for connecting electrodes of said semiconductor chip and said wiring board by metal thin wires; and
- a step for sealing said second adhesive layer and part of said semiconductor chip with a first

encapsulating resin and sealing said metal thin wires and said semiconductor chip with a second encapsulating resin after said first encapsulating resin has been cured.

6. The method as claimed in claim 5, wherein said first encapsulating resin and said second encapsulating resin are respectively encapsulating resins different in material from each other.

7. A method of manufacturing a semiconductor device, comprising the following steps:

a step for preparing a heat spreader;

a step for forming a first adhesive layer and a second adhesive layer over a principal surface of said heat spreader;

a step for forming a wiring board over said first adhesive layer;

a step for forming a semiconductor chip over said second adhesive layer;

a step for connecting electrodes of said semiconductor chip and said wiring board by metal thin wires;

a step for sealing said second adhesive layer and part of said semiconductor chip with an encapsulating resin; and

a step for sealing said metal thin wires and said semiconductor chip with said encapsulating resin after

said encapsulating resin has been cured.

ABSTRACT OF THE DISCLOSURE

A recessed portion of an adhesive is formed between a wiring board and a heat spreader. Voids occur in the neighborhood of the top of each metal thin wire upon curing an encapsulating resin, thus causing a reduction in moisture resistance. Therefore, the present invention provides a semiconductor device wherein a semiconductor chip and a wiring board are fixed to a heat spreader by an adhesive layer formed over a principal surface of the heat spreader, by using a method such as thermocompression bonding to thereby eliminate a recessed portion, and the parts are sealed with an encapsulating resin inclusive of the semiconductor chip and the metal thin wires.

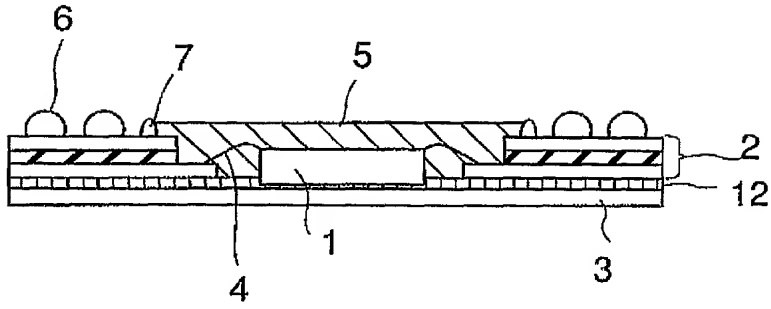
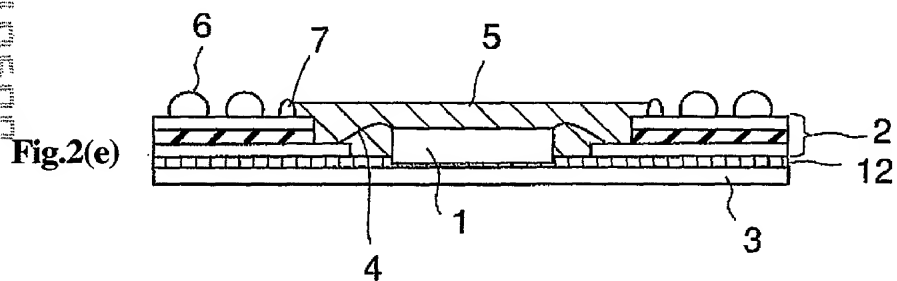
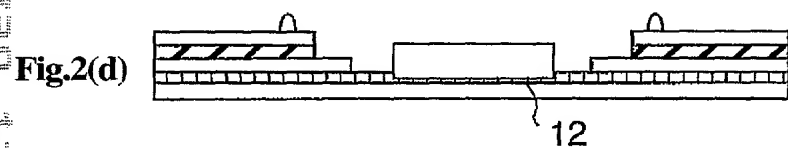
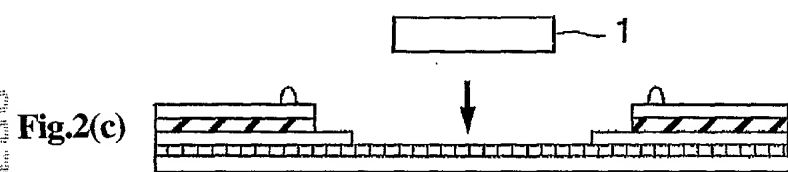
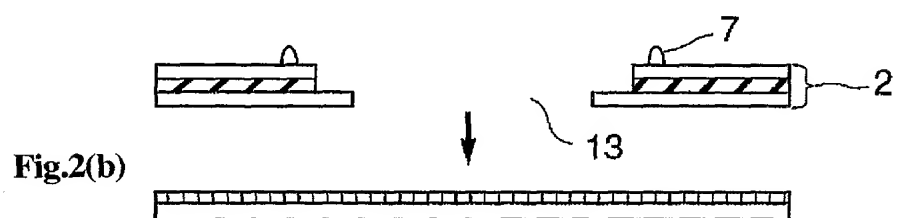
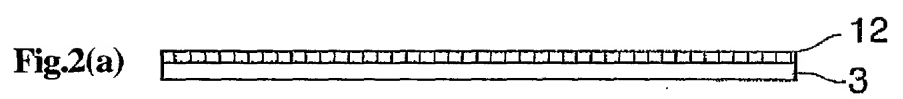


Fig. 1

00507 625060



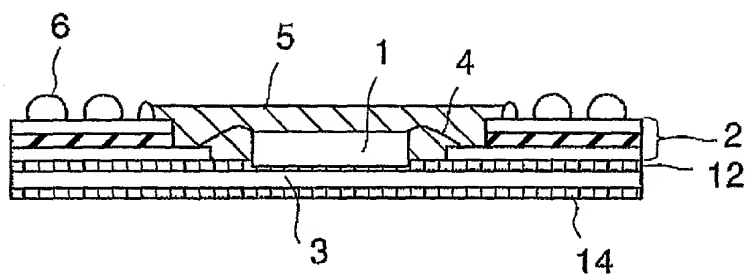
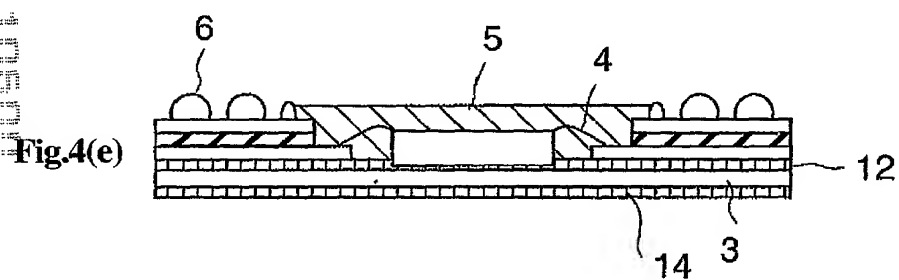
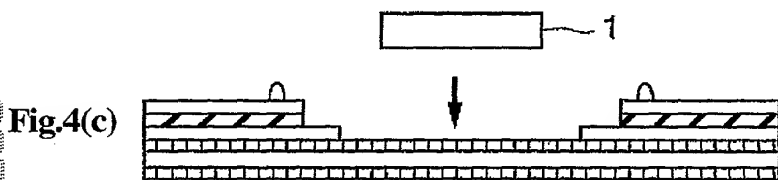
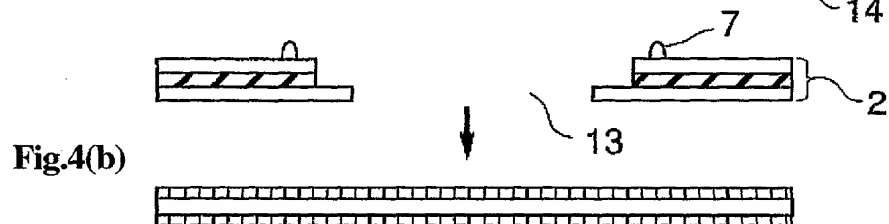
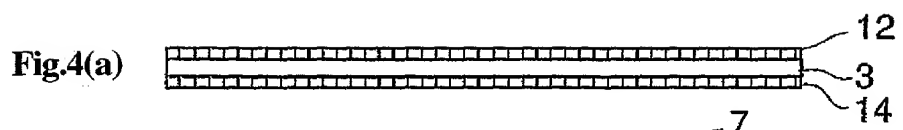


Fig.3



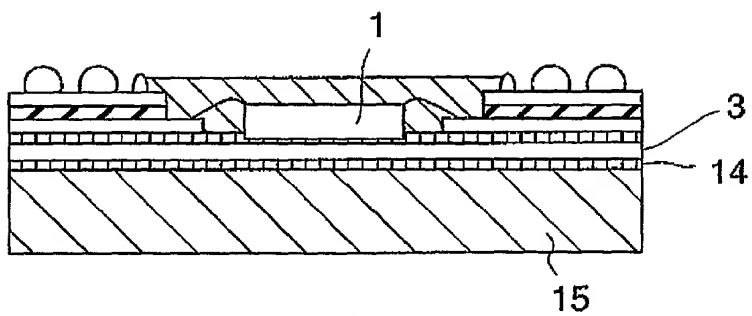
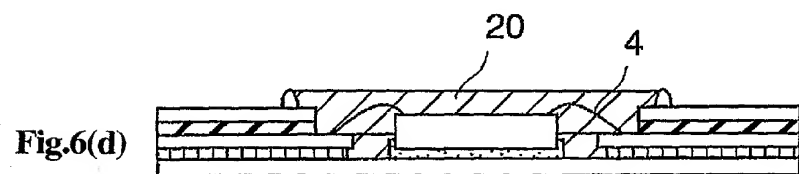
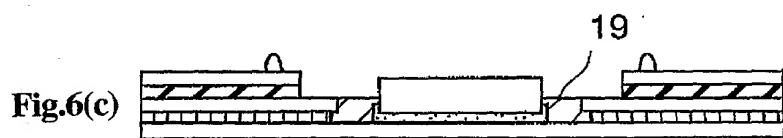
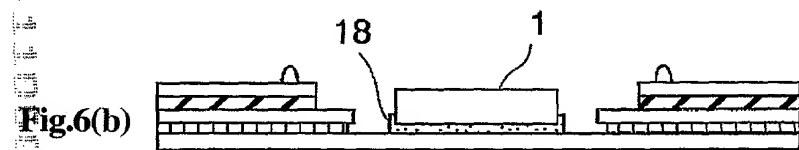
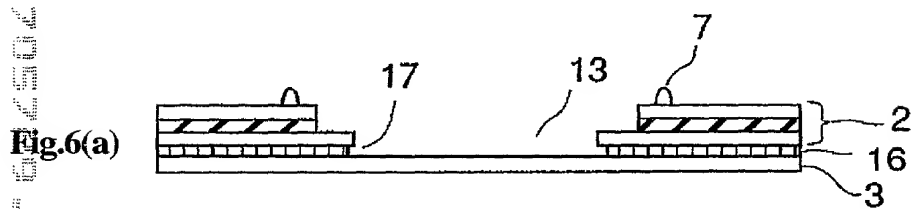


Fig.5

Downloaded from ascelibrary.org by Seattle University on 06/01/15



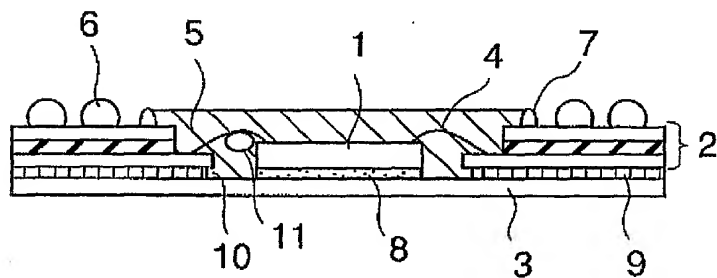
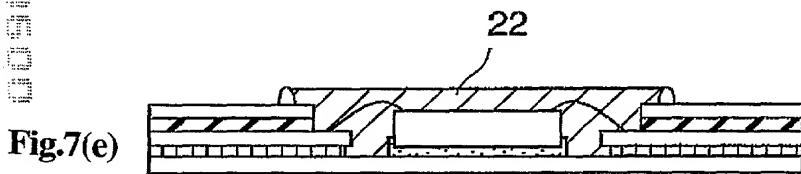
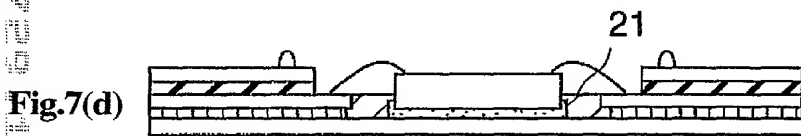
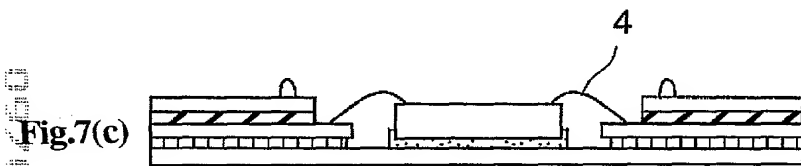
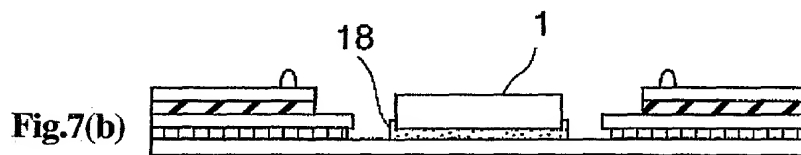
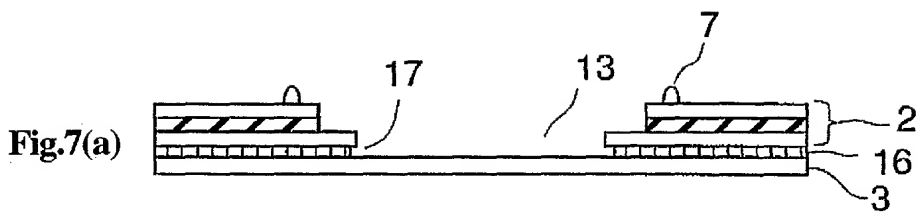


Fig.8

Declaration and Power of Attorney For Patent Application**特許出願宣言書及び委任状****Japanese Language Declaration****日本語宣言書**

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SEMICONDUCTOR DEVICE AND METHOD

OF MANUFACTURING THE SAME

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ 月 日に提出され、米国出願番号または特許協定条約
国際出願番号を _____ とし、
(該当する場合) _____ に訂正されました。

☐ was filed on _____
as United States Application Number or
PCT International Application Number
_____ and was amended on
_____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above

私は、連邦規則法典第37編第1条56項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Japanese Language Declaration

(日本語宣言書)

私は、米国法典第35編119条(a)-(d)項又は365条(b)項に基づき下記の、米国以外の国の少なくとも一カ国を指定している特許協力条約365(a)項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

Prior Foreign Application(s)

外国での先行出願

| | |
|-------------|-----------|
| 320442/1999 | JAPAN |
| (Number) | (Country) |
| (番号) | (国名) |

| | |
|----------|-----------|
| (Number) | (Country) |
| (番号) | (国名) |

私は、第35編米国法典119条(e)項に基づいて下記の米国外特許出願規定に記載された権利をここに主張いたします。

| | |
|-------------------|---------------|
| (Application No.) | (Filing Date) |
| (出願番号) | (出願日) |

私は、下記の米国法典第35編120条に基づいて下記の米国外特許出願に記載された権利、又は米国を指定している特許協力条約365条(c)に基づく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第35編112条第1項又は特許協力条約で規定された方法で先行する米国外特許出願に開示されていない限り、その先行米国外出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第37編1条56項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

| | |
|-------------------|---------------|
| (Application No.) | (Filing Date) |
| (出願番号) | (出願日) |

| | |
|-------------------|---------------|
| (Application No.) | (Filing Date) |
| (出願番号) | (出願日) |

私は、私自身の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じているところに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第18編第1001条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行えば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365 (b) of any foreign application(s) for patent or inventor's certificate, or 365 (a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent of inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Priority Not Claimed

優先権主張なし

| | |
|------------------------|--------------------------|
| 11-Nov-99 | <input type="checkbox"/> |
| (Day/Month/Year Filed) | |

| | |
|------------------------|--------------------------|
| (Day/Month/Year Filed) | <input type="checkbox"/> |
| (出願年月日) | |

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

| | |
|-------------------|---------------|
| (Application No.) | (Filing Date) |
| (出願番号) | (出願日) |

I hereby claim benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

| |
|--|
| (Status: Patented, Pending, Abandoned) |
| (現況: 特許許可済、係属中、放棄済) |

| |
|--|
| (Status: Patented, Pending, Abandoned) |
| (現況: 特許許可済、係属中、放棄済) |

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and the such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Japanese Language Declaration (日本語宣言書)

委任状： 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。(弁護士、または代理人の氏名及び登録番号を明記のこと)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (*list name and registration number*)

Steven M. Rabin (Reg. No. 29,102), Thomas M. Champagne (Reg. No. 36,478), Robert H. Berdo, Jr. (Reg. No. 38,075)
and David S. Lee (Reg. No. 38,222)

書類送付先

Send Correspondence to:

RABIN & CHAMPAGNE, P.C.,
1101 14th Street, Suite 500, Washington, D.C. 20005

直接電話連絡先： (名前及び電話番号)

Direct Telephone Calls to: (*name and telephone number*)

Steven M. Rabin
RABIN & CHAMPAGNE, P.C.

Telephone: (202) 659-1915, Fax: (202) 659-1898

| | | | |
|--|---------------------|--|------|
| 唯一または第一発明者名 | | Full name of sole or first inventor | |
| Yoshinori SHIZUNO | | | |
| 発明者の署名 | 日付 | Inventor's signature | Date |
| <i>Y. Shizuno</i> | | <i>October 30, 2000</i> | |
| 住所 | Residence | | |
| Kanagawa | , Japan | | |
| 国籍 | Citizenship | | |
| Japanese | | | |
| 私書箱 | Post Office Address | | |
| c/o Oki Electric Industry Co., Ltd. | | | |
| 7-12, Toranomom 1-chome, Minato-ku, Tokyo, Japan | | | |
| 第二共同発明者名 | | Full name of second joint inventor, if any | |
| | | | |
| 第二共同発明者の署名 | 日付 | Second inventor's signature | Date |
| | | | |
| 住所 | Residence | | |
| | , Japan | | |
| 国籍 | Citizenship | | |
| | | | |
| 私書箱 | Post Office Address | | |
| | | | |

(第三以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for third and subsequent joint inventors.)